## What is claimed is:

[Claim 1] 1. A method of operating dynamic random access memory (DRAM) using a bit line and a bit line bar, wherein a charge storage device of the DRAM is adapted for storing data, the charge storage device is coupled to the bit line via a switch device, the method comprising:

programming the charge storage device with a first or a zero voltage, wherein when the switch device is turned on, a switch voltage drop generated in the switch device, and the first voltage equals to a voltage obtained by subtracting the switch voltage drop from a power voltage; and

accessing the data stored in the charge storage device, wherein the step of accessing the data comprises:

charging the bit line and the bit line bar to the power voltage;

turning on the switch device; and

determining the data stored in the charge storage device according to a voltage difference between the bit line and the bit line bar.

[Claim 2] 2. The operating method of DRAM of claim 1, further comprising a step of pulling down a voltage of the bit line bar a preset voltage before determining the data stored in the charge storage device.

[Claim 3] 3. The operating method of DRAM of claim 2, wherein the preset voltage is one half of the voltage drop on the bit line while the switch device is turned on after the charge storage device is programmed by the zero voltage.

[Claim 4] 4. The operating method of DRAM of claim 1, wherein turn-on/turn-off of the switch device is controlled by a word line, and the word line turns on the switch device with the power voltage.

[Claim 5] 5. A writing operation of a dynamic random access memory (DRAM) using a bit line and a bit line bar, wherein a charge storage device of the DRAM is adapted for storing data and is coupled to the bit line via a switch device, the writing operation comprising:

turning on the switch device; and
programming the charge storage device with a first voltage or a zero voltage, wherein the first voltage equals to a voltage obtained by subtracting a switch voltage drop from a power voltage, and the switch voltage drop is a voltage drop generated in the switch device when the switch device is turned on.

[Claim 6] 6. The writing method of DRAM of claim 5, wherein turn-on/turn-off of the switch device is controlled by a word line, and the word line turns on the switch device using the power voltage.

[Claim 7] 7. A reading operation of a dynamic random access memory (DRAM) using a bit line and a bit line bar, wherein a charge storage device of the DRAM is adapted for storing data and is coupled to the bit line via a switch device, the reading operation comprising:

charging the bit line and the bit line bar to a power voltage;
turning on the switch device; and
determining the data stored in the charge storage device according to a voltage difference between the bit line and the bit line bar, wherein the power voltage controls turn-on/turn-off of the switch device.

[Claim 8] 8. The reading method of DRAM of claim 7, further comprising a step of pulling down a voltage of the bit line bar a preset voltage before determining the data stored in the charge storage device.

[Claim 9] 9. The reading method of DRAM of claim 8, wherein the preset voltage is one half of the voltage drop on the bit line while the

switch device is turned on after the charge storage device is programmed by the zero voltage.

[Claim 10] 10. The reading method of DRAM of claim 7, wherein turn-on/turn-off of the switch device is controlled by a word line.